CLAIMS:

1. A bus system for an integrated circuit device, the bus comprising a plurality of bus lines (4) each of which connects a driver circuit (2) and a receiver circuit (6), characterized in that each receiver circuit comprises:

- a first detector (10) operably connected to receive a data signal from an associated bus line (4), and operable to detect a rising transition of the data signal with respect to a first threshold level, and to produce a first output signal upon detection of such a rising transition;
- a second detector (12) operably connected to receive the data signal, and operable to detect a falling transition of the data signal with respect to a second threshold level, and to produce a second output signal upon detection of such a transition; and
- output means operable to output the first or second output signal as a receiver output signal.

2. A bus system as claimed in claim 1, wherein the output means comprises a multiplexer (14) operably connected to receive the first and second output signals, and operable to output the receiver output signal in dependence upon a previous receiver output signal.

3. A bus system as claimed in claim 1 or 2, wherein the first and second threshold levels are variable.

4. A bus system as claimed in claim 3, further comprising a calibrator (18) for adjusting the first and second threshold levels.

5. A bus system as claimed in claim 4, wherein the first and second detectors (10,12) include respective pluralities of transistors, and the calibrator (18) is operable to activate varying numbers of those transistors, in order to adjust the threshold levels.

6. A bus system as claimed in claim 4 or 5, further comprising a glitch sensor circuit 28) which is operable to detect glitches on at least one of the bus lines (4).

7. A bus system as claimed in claim 6, wherein the glitch sensor circuit (28) comprises a pair of latches (30,32) each having an output, and a multiplexer (34) operable to select one of the latch outputs for supply to the calibrator (18).

8. A bus system as claimed in claim 6 or 7, wherein the calibrator (18) is operable to supply test signals to the bus lines, and the glitch sensor circuit (28) is operable to detect glitches on at least one bus line (4) and to supply a glitch signal to the calibrator (18), the calibrator (18) then being operable to adjust the threshold values of the detectors in dependence upon the glitch signal.

9. A bus system as claimed in claim 6 or 7, further comprising a test bus including a plurality of test drivers (22), and corresponding pluralities of bus lines (24) and receivers (26), the calibrator (18) being operable to supply test signals to the test bus lines (24), and the glitch sensor circuit (28) being operable to detect glitches on the test bus lines (24) and to supply a glitch signal to the calibrator (18), the calibrator then being operable to adjust threshold values of the detectors in dependence upon the glitch signal.

10. A method of operating a bus system for an integrated circuit device, the bus comprising a plurality of bus lines (4) each of which connects a driver circuit (2) and a receiver circuit (6), characterized in that the method comprises:

- receiving a data signal from a bus line (4);
- detecting a rising or falling transition of the data signal with respect to first and second threshold levels respectively;
- producing a first output signal upon detection of a rising transition, or producing a second output signal upon detection of a falling transition; and
- outputting the first or second output signal as a receiver output signal.

11. A method as claimed in claim 10, wherein the first or second output signal is output a multiplexer (14) operably connected to receive the first and second output signals, and operable to output the receiver output signal in dependence upon a previous receiver output signal.

12. A method as claimed in claim 10 or 11, wherein the first and second threshold levels are variable.

13. A method as claimed in claim 12, further comprising adjusting the first and second threshold levels.

14. A method as claimed in claim 13, wherein the first and second detectors (10,12) include respective pluralities of transistors, and the threshold levels are adjusted by activating varying numbers of those transistors.

15. A method as claimed in claim 13 or 14, further comprising detecting glitches on at least one of the bus lines (4).

16. A method as claimed in claim 15, wherein glitches are sensed using glitch sensor circuit (28) which comprises a pair of latches (30,32) each having an output, and a multiplexer (34) operable to select one of the latch.

17. A method as claimed in claim 15 or 16, further comprising supplying test signals to the bus lines, detecting glitches on at least one bus line (4), and adjusting the threshold values in dependence upon detected glitches.

18. A method as claimed in claim 15 or 16, further comprising supplying test signals to test bus lines (24), detecting glitches on the test bus lines (24), and adjusting the threshold values in dependence upon detected glitches.